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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,938	10/14/2004	Hong-Gee Fang	14001-US-PA	5937

31561 7590 02/27/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/711,938	FANG ET AL.
	Examiner	Art Unit
	Thong Q. Le	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on August 30, 1999 has been entered.

2. Claims 1-10 are presented for examination.

Drawings

3. The drawings were received on 01/23/2006. These drawings are Figures 1-2.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kirihata et al. (U.S. Patent No. 6,829,682).

Regarding claim 1, Kirihata et al. disclose a method of operating (DRAM) (ABSTRACT) using a bit line (Figure 2A, BL) and a bit line bar (Figure 2A, /BL), wherein a charge storage device (Figure 2A, 106) of the DARM ((Figure2A, 102) is adapted for storing data, the charge storage device is coupled to the bit line ((Figure 2A), via a switch device (Figure 2A, 104), the method comprising:

programming the charge storage device with a first or a zero voltage (Column 2, lines 40-44) , wherein when the switch decide is turned on, a switch voltage drop generated in the switch device and the first voltage equals to a voltage obtained by subtracting the switch voltage drop from a power voltage (Column 3, lines 20-23, ; and

accessing the data stored in the charge storage device, wherein the step of accessing the data comprises:

charging the bit line and bit line bar to the power voltage (column 2, lines 40-52);

turning on the switch device (Column 3, lines 20-26); and

determining the data in the charge storage device according to a voltage difference between the bit line and the bit line bar (Column 2, lines 40-52).

Regarding claims 2-3, Kirihata et al. disclose a step of pull down a voltage of bit line bar a preset voltage before determining the data stored in the charge storage device Column 3, lines 20-28), and wherein the preset voltage is about one half of the voltage drop on the bit line while the switch device is turned on after the charge storage is programmed by the zero voltage (Column 3, lines 20-38).

Regarding claim 4, Kirihata et al. disclose wherein turn-on/turn-off of the switch device is controlled by a word line and the word line turns on the switch device with the power voltage (Figure 2A, WL, Column 2, lines 47-49, Column 3, lines 20-23).

Regarding claim 5, Kirihata et al. disclose a writing operation of (DRAM) (Figure 2A, 102) using a bit line (BL) and a bit line bar (/BL), wherein a charge storage device of the DRAM is adapted to storing data and is coupled to the bit line via a switch device, the writing operation comprising turning on the switch device (Column 3, lines 15-20), programming the charge storage device with a first voltage or a zero voltage, wherein the first voltage equals to a voltage obtained by subtracting a switch voltage drop from a power voltage, and the switch voltage drop is a voltage drop generated in the switch device when the switch device turn on (Column 2, lines 40-49, Column 3, lines 14-38).

Regarding claim 6, Kirihata et al. disclose wherein turn-on/turn-off of the switch device is controlled by a word line and the word line turns on the switch device with the power voltage (Figure 2A, WL, Column 2, lines 47-49, Column 3, lines 20-23).

Regarding claims 7-10, Kirihata et al. disclose a writing operation of (DRAM) (Figure 2A, 102) using a bit line and a bit line bar (Figure 2A, BL, /BL) , wherein a charge storage device of the DRAM is adapted to storing data and is coupled to the bit line via a switch device, the read operation comprising charging the bit line and the bit line bar to power voltage (Column 3, lines 17-18), turning on the switch device (Column 3, line 20), determining the data stored in the charge storage device according to a voltage difference between the bit line and the bit line bar, wherein the power voltage controls turn-on-turn-off of the switch device (Column 3, lines 22-27), and a step of pull

down a voltage of the bit line bar a preset voltage before determining the data stored in the charge storage device (Column 3, lines 26-27), and wherein the preset voltage is about one half of the voltage drop on the bit line while the switch device is turned on after the charge storage device is programmed by the zero voltage (Column 3, lines 22-38) and wherein turn-on/turn-off of switch device is controlled by word line (Column 3, lines 20-23).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827